EMC Filter Design at the Push of a Button
PowerUP: The Next Step in the Evolution of Power Electronics

This year’s PowerUP Expo Virtual Conference has seen many speakers talking about wide-bandgap (WBG) semiconductors, energy trends, and low-power aspects. Efficiency is a driving force in all industrial sectors, including consumer. Thanks to their savings in size, weight, and cost, as well as higher efficiency, gallium nitride and silicon carbide power devices are making major advances beyond several applications. In the last couple of decades, the worldwide SiC and GaN scenes have been characterized by development and growing industry acceptance. Meanwhile, other semiconductor devices serve the needs of motor drive and power control. As efficiency standards for these applications improve, cost-effective and energy-efficient control solutions, test and measurement solutions, and transducers/sensors simplify design and provide a high level of integration, as well as enhanced safety features and certified isolation capabilities. In this issue, we propose several topics, with a section about PowerUP regarding the proceedings. Electromagnetic-compatibility (EMC) compliance is often the last hurdle that an electronic device has to overcome in the development process. It is not rare at all for circuit-specific and layout-specific changes to be required in the process. Gerhard Stelzer, senior technical editor at Würth Elektronik eiSos, analyzes the new EMI Filter Designer, which can be used to design EMC filters for conducted differential-mode interference signals. The emergence of cloud-based internet services has initiated a strong growth of processing power, creating a clear need for highly efficient and compact server power supplies. We will analyze how to meet the design requirements of power supplies using silicon and WBG switches. The main topics of the PowerUP proceedings are WBG manufacturing and design features. We summarize key aspects of SiC fabrication technology and outline non-CMOS-compatible processes that have been streamlined to allow for mass SiC device fabrication in conventional mature Si fabs. GaN has become the de facto material in third-generation semiconductors. However, making GaN wafers in the quality you need and the thermal resistance you desire are challenges that fabs are still trying to overcome. Moreover, we’re dealing with a potentially more serious issue: climate change. As the world advances toward a sustainable, greener future, many countries are powering down fossil-fuel energy generation in favor of renewables. Industry areas such as energy, mobility, and manufacturing are important to environmental success. Disruptions in various areas are required to decrease, control, and manage the emissions problem. All talks are available on-demand by the PowerUP platform at [www.powerup-expo.com](http://www.powerup-expo.com).

Yours Sincerely,
Maurizio Di Paolo Emilio
Editor-in-Chief, Power Electronics News
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EMC Filter Design at the Push of a Button

*EMC compliance of a product is annoying but unavoidable. At the same time, EMC filter design is far from trivial. The new REDEXPERT filter designer tool simplifies filter design, helping to save time and money.*

*By Gerhard Stelzer, senior technical editor at Würth Elektronik eiSos*

Electromagnetic compatibility (EMC) compliance is often the last hurdle that an electronic device has to overcome in the development process. It is not rare at all for circuit-specific and layout-specific changes to be required in the process. These then extend the product development cycle and increase costs. For this reason, Würth Elektronik now offers the new EMI Filter Designer as part of its REDEXPERT tool family, which can be used to design EMC filters for conducted differential-mode interference signals.

A typical application is an input filter for DC/DC converters, especially switching regulators, which can generate a lot of interference. In the same way, filters for attenuating broadband interference in
other applications can be calculated. The goal of a filter circuit is to realize a defined insertion loss in the selected frequency range. This is achieved with a high impedance over the desired frequency range by the largest possible mismatch between load and source. Here, the insertion loss \( a \) in Equation 1 is defined as the ratio of the voltage without filter compared with the same circuit with a filter. For a second-order LC filter, Equation 2 applies to the cutoff frequency \( f_c \).

Equation 1
\[
\alpha = 20 \times \log\left(\frac{U_{\text{load1}}}{U_{\text{load2}}}\right)
\]

Equation 2
\[
f_c = \frac{1}{2\pi\sqrt{LC}}
\]

However, Equation 2 assumes ideal components. The inductance does not take into account the winding resistance or the capacitance between the windings, and for the capacitor the equivalent series resistance (ESR) and the equivalent series inductance (ESL), etc.

REDEXPERT EMI FILTER DESIGNER
REDEXPERT EMI Filter Designer takes these parasitic elements into account in the frequency range up to 30 MHz, so the simulation much more accurately reflects the real electrical behavior of the components and the filter characteristics up to fourth order.

The EMI Filter Designer determines the most suitable topology as a suggestion from the input variable's operating voltage, current, load/line impedance stabilization network and interference source impedance, cutoff frequency, and attenuation at a defined frequency.

A total of six topologies are available for filters from second to fourth order: LC, CL, Pi (CLC), T (LCL), LC-LC, and CL-CL.

After selecting the topology, the software calculates the discrete component values and simulates the frequency responses of gain, input impedance, and output impedance of the filter. A summary again shows the input values, the circuit, a BOM with an ordering function, and the simulated frequency responses. The calculation and the following automatic selection of the component values is based on a Butterworth characteristic with the corresponding position of the poles.

PRACTICAL EXAMPLE WITH REDEXPERT EMI FILTER DESIGNER
REDEXPERT EMI Filter Designer is an online tool at www.we-online.com/filter-designer that is suitable for designing an input or output filter for AC/DC or DC/DC converters, etc. A typical input filter for a DC/DC converter is shown in Figure 1. The main goal of the filter tool is to calculate a clean signal attenuation for defined input parameters by achieving maximum impedance mismatch.

ASYMMETRICAL INPUT FILTER FOR DC/DC CONVERTERS
A good filter design requires the most accurate input specifications possible. In reality, DC/DC
converters have a bulk capacitor in parallel with the input impedance on the input side, so it is common to take the ESR as the input impedance. The ESR value is usually in the range of 0.1 Ω to 1 Ω.

For example, if we use the WCAP-AS5H 865230557007 from Würth Elektronik as the bulk capacitor, then the ESR value is 100 mΩ. If we now want to achieve a filter characteristic with an attenuation of 35 dB at 350 kHz, the tool recommends a CL circuit (Figure 2) and determines the values of the components to be $C_1 = 47.0 \, \mu\text{F}$ and $L_1 = 240 \, \text{nH}$. Figure 3 also shows the frequency response of attenuation, input impedance, and output impedance.

**OUTPUT FILTER FOR DC/DC CONVERTERS**

Due to the high switching frequencies commonly used in DC/DC converters today, an output filter is required to reduce high-frequency noise and ripple. For example, the output voltage might have a
ripple component of 50 mV at 1 MHz, which needs to be reduced to 15 mV. The required attenuation ($a$) in decibels is obtained according to Equation 3.

$$a = 20 \times \log \left( \frac{50 \text{ mV}}{15 \text{ mV}} \right) = 10.5 \text{ dB}$$

With the input parameters “Attenuation 11 dB” and “at Frequency 1 MHz” and the choice of the output filter as LC combination with the input parameters “Load Impedance = 50 Ω/Noise Source Impedance = 0.1 Ω,” the tool now recommends an LC topology with $L_1 = 55 \text{ nH}$ and $C_1 = 4.7 \text{ µF}$. With regard to the topology, it should be noted that the noise source is always on the right side of the specified filter and the load on the left (Figure 1); i.e., the filter must be integrated in the corresponding circuit in such a way that the inductance is located directly at the DC/DC converter and the capacitor in parallel to the load.

Reference

▶ REDEXPERT EMI Filter Designer
The AspenCore Guide to Silicon Carbide

Silicon Carbide (SiC), a wide-bandgap semiconductor, is driving a profound transformation of power electronics and clean energy systems. This 145-page guide offers a detailed analysis of the market trends and an in-depth discussion of key aspects of SiC power technology.
Developing engineers are faced with a challenge when it comes to the choice of a suitable cooling concept for power electronics. This is particularly the case with flat housings, where corresponding know-how is required. Thought should be given to this issue during the concept phase, as it may prove difficult to solve this problem if there is very little space for dissipating heat. SEPA EUROPE has developed a smart solution for such requirements — namely, the HZ210, an in-house development that is available in different dimensions. SEPA EUROPE has developed the new high-performance active heat sink HZ210 using the powerful LY60B radial fan. The case study achieved an impressively low thermal resistance of 0.5 K/W during laboratory testing. With an overall height of a mere 25 mm, this opens up new possibilities for developers to enable the cooling of power components in flat housings. In the event that a temperature increase of 40 K is allowed, 80-W power loss can be reliably dissipated. The cooling system comprising SEPA blower, extruded heat sink, and cover plate keeps the noise at a comfortably low level. The microphone recorded no more than 34 dB(A) in the anechoic chamber. The fan is available in 5-V and 12-V versions and has a service life of 210,000 hours (MTBF) at 40°C thanks to its reliable MagFix® sleeve bearing.
Packaging and Thermal Solutions to Fulfill Trends in Data Centers and Server SMPS

How to meet the design requirements of power supplies using silicon and wide-bandgap switches

By Daniel Hölzl, package concept engineer, and Sam Abdel-Rahman, system architect for server/data center SMPS, both at Infineon Technologies

The emergence of cloud-based internet services, artificial intelligence, and cryptocurrency has initiated a strong growth of processing power in data centers worldwide. In combination with rising electricity and real estate prices, this trend creates a clear need for highly efficient and compact server power supplies.
To achieve the required higher power density, the following three main contributors must be considered:

▶ **Increased efficiency** to maintain an acceptable total power loss in a given volume. This drives the transition to new topologies and technologies. A great example is the transition from the conventional silicon classic-boost PFC to the gallium nitride/silicon carbide totem-pole PFC.

▶ **Improved packages and thermal solutions** that can dissipate the power away from the device junction to heatsinks and ambient. This becomes more challenging in smaller surface-mount device (SMD) packages that are the main enabler for high-density converters.

▶ **Optimized system design and switching frequency** to achieve maximum density without violating efficiency requirements or temperature-rise limits. This leads to an increased switching frequency, driving the transition from conventional to new packages and thermal solutions.

Typically, state-of-the-art, high-efficiency power supplies are comprised of a bridgeless PFC stage, such as a totem-pole stage, and a resonant DC/DC stage, such as an LLC converter (see Figure 1). An example specification of a server supply is $V_{in} = 180–277$ V, $V_{out} = 48$ V, $P_{out} = 3$ kW.

To quantify the achievable performance tradeoff between efficiency and power density, the Pareto optimization method is applied. This method systematically considers all available degrees of freedom in the design of the different converter systems. By employing detailed system and component models, it identifies the optimal designs positioned on the Pareto front. The efficiency is calculated for 50% of the rated output power and includes both PFC and LLC stage losses.

The Pareto front for the entire server supply system is calculated, and the optimization results are shown in Figure 2. The graph indicates that efficiencies close to 98.2% can be achieved for medium power densities (~40 W/in.$^3$), while designs with more than 80 W/in.$^3$ have efficiencies below 97.5%. Another important observation from this figure is the higher switching frequency of the LLC stage required for higher-density designs. These observations confirm the necessity of packages operating at a higher frequency with higher efficiency.
SMD PACKAGES USED IN SMPS TOPOLOGIES

Infineon offers a larger portfolio of bottom-side cooling (BSC) and top-side cooling (TSC) packages that fulfill the higher-power and higher-density trends in server switch-mode power supply (SMPS) applications. This section discusses and compares the different packages concerning topics such as assembly, thermal performance, and electrical parasitics.

ASSEMBLY IMPLEMENTATIONS OF BSC AND TSC PACKAGES

**Bottom-side cooling**

Figures 3 and 4 show the principal cooling concept for BSC and TSC. In both cases, the SMD package is mounted on the PCB, usually via a reflow-soldering process. For BSC, the main heat flux is directed from the device heatsink (exposed pad) on the bottom of the package through the PCB to an external heatsink mounted on the opposite side of the PCB. Therefore, thermal vias below the package and through the PCB are needed for heat transfer when using an FR4-based PCB. On the backside of the PCB, the external heatsink is mounted on the area with the thermal vias. The heatsink and the PCB are electrically separated via a thermal interface material (TIM). Quite often, a foil with a thickness in the range of 100–500 μm is used as TIM, which has, in the best case, a good thermal admittance ($\lambda$). This leads ideally to a low thermal impedance ($Z_{th, ja}$) for the overall system.
The PCB has a certain thickness, influenced by the number of necessary Cu layers for circuit design and a density limitation for the thermal vias. Because of that, the effective cross-sectional area for heat transfer through the PCB is reduced compared with the area for heat transfer offered by the device heatsink. This is the first bottleneck. The second bottleneck is the TIM, having a much lower $\lambda$ than the device heatsink and the external heatsink.

In some cases, replacing the FR4-based substrate with insulated metal substrate (IMS) allows for a higher heat flux without exceeding the maximum device or PCB temperature. Especially for single-layer PCB designs, neither thermal vias nor additional TIM are needed. The external heatsink can be saved because the aluminum core of the board is used as a heatsink. However, although $Z_{thja}$ is reduced, the number of temperature cycles on board (TCoB) is reduced, especially for non-leaded SMD packages like TO-leadless (TOLL) or ThinPAK caused by the rigid IMS-based PCB compared with the more flexible FR4-based PCB.

**Top-side cooling**

In TSC packages, the device heatsink on top of the package is interfaced directly to the external heatsink through the TIM (Figure 4). In this case, there is no heat passing through the PCB and thermal vias therefore eliminating their thermal impedance from the total thermal impedance. This leads to enhanced thermal conductivity and higher package maximum power dissipation.

Moreover, another advantage of TSC packages is the free area on the opposite PCB side that can be used to place other devices such as gate drivers and passive components, as well as space for signal routing directly below the package body.

For a good thermal interface, it is recommended to press the heatsink with a certain force on the TSC device. In the case of leaded SMD packages with a positive package standoff (Figure 5, left), this force and other temperature-cycling–induced forces are absorbed by the package leads, resulting in very good TCoB of 2,000 cycles in the case of QDPAK.
In case of a negative package standoff (Figure 5, right), other considerations are needed for the PCB design to avoid system reliability issues, which could cause additional effort and complexity for the system design and manufacturing. A negative package standoff has the advantage of reduced $Z_{thj}$ because of its reduced package height tolerance, leading to a thinner TIM thickness. However, when considering other tolerances like PCB warpage, especially with larger PCB size and multiple power devices using a common heatsink, the thermal advantage of a negative package standoff becomes less important.

For the common heatsink approach, Figure 6 shows schematically the TIM stack between device and heatsink, which consists of insulation foil and gap filler in this example. The gap filler is used for compensating device-, heatsink-, and PCB-related manufacturing tolerances. Using only a gap filler for heat transfer, a reliable insulation between the device and external heatsink must be ensured. Additionally, the gap filler material must fulfill the necessary breakdown rating, and enclosed particles within the gap filler or blowholes during PCB assembly need to be prevented. In general, a clean manufacturing ambient for PCB assembly can lower the risk of system failures caused by pollution during system manufacturing.
For further improved \(Z_{\text{thja}}\) and dynamic power dissipation for TSC, the implementation of an intermediate heat spreader is a good option, as shown in Figure 7. The thermal capacity of this additional heatsink can store for a certain time (some seconds) the additional heat and transfer it further to the common heatsink and ambience. Depending on the system design, removing the common heatsink and TIM is also possible for improved system \(Z_{\text{thja}}\), wherein the heat spreader is the primary heatsink and is directly cooled by the fan airflow.

**Figure 7: Single-device heat-spreader mounting**

\(Z_{\text{thja}}\) time-dependent plots for selected through-hole device (THD), BSC SMD, and TSC SMD packages considering an FR4-based PCB design with forced air cooling. The same device inside all shown packages is assumed just as the same power losses. Comparing DDPAK (TSC package) with TO263 (BSC package) on an FR4-based PCB, DDPAK achieves 60% lower \(Z_{\text{thja}}\), although the effective cooling area of both packages is quite similar. DDPAK bypasses the bottleneck “thermal vias,” as described in the section before. The graph also illustrates that top-side packages

**Figure 8: Typical transient thermal impedance junction ambient (\(Z_{\text{thja}}\)) for multiple packages at forced convection**

**Thermal performance**

Figure 8 shows \(Z_{\text{thja}}\) time-dependent plots for selected through-hole device (THD), BSC SMD, and TSC SMD packages considering an FR4-based PCB design with forced air cooling. The same device inside all shown packages is assumed just as the same power losses. Comparing DDPAK (TSC package) with TO263 (BSC package) on an FR4-based PCB, DDPAK achieves 60% lower \(Z_{\text{thja}}\), although the effective cooling area of both packages is quite similar. DDPAK bypasses the bottleneck “thermal vias,” as described in the section before. The graph also illustrates that top-side packages
can achieve $Z_{thja}$ values comparable to THDs. The legend shows that using thin layers of isolation materials with a comparable high $\lambda$ is the key to achieving good $Z_{thja}$ results. Beyond that, using gap filler and isolation foil with further higher $\lambda$ will lead to a situation whereby the shown TSC packages deliver lower $Z_{thja}$ than the THD.

**Low inductance parasitic advantage in high-frequency operation**

Figure 9 demonstrates the effect of package source inductance ($L_{Sc}$) on the turn-on transient. $L_{Sc}$ is increased from 0 to 4 nH. The rise of drain current (di/dt) causes an inductive voltage drop over $L_{Sc}$, which subtracts from gate drive voltage and thus reduces the gate current. So the voltage transient takes longer, and the losses increase. The same mechanism but in an opposite manner applies to the turn-off transient.

![Figure 9: Example of package source inductance effect on switching on: waveform details (left) and losses (right)](image)

**Table 1: Overview of THD and SMD BSC and TSC packages for server applications. For assessment of package inductance, a device with a similar $R_{DS(on)}$ inside the package is assumed**

<table>
<thead>
<tr>
<th></th>
<th>Bottom-side cooling</th>
<th>Top-side cooling</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TO247</td>
<td>D’PAK</td>
</tr>
<tr>
<td>Creepage distance [mm]</td>
<td>2.5</td>
<td>4.2 &amp; 5.8</td>
</tr>
<tr>
<td>Thermal performance</td>
<td>best</td>
<td>good</td>
</tr>
<tr>
<td>Package inductance [mm]</td>
<td>low</td>
<td>lower</td>
</tr>
<tr>
<td>Kelvin source</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Package stand-off</td>
<td>–</td>
<td>positive</td>
</tr>
</tbody>
</table>

Device reference: IPW60R060C7, IMBG65R057M1H, IG60R070D1, IPT60R055CFD7, IPL60R065C7, IGOT60R070D1, IPD6D0R055CFD7, IPDQ60R055CFD7
The negative effect of $L_{Sc}$ discussed above can be eliminated by using a separate source sense pin (Kelvin source) for controlling the gate (Figure 10, right), which effectively reduces switching losses. By using the source sense connection to drive the gate, the $L_{Sc}$ comes outside the gate drive loop. Therefore, its induced voltage peaks will not feed back into the driving circuit as would happen in the standard configuration (Figure 10, left) with only a single source connection to the MOSFET.

![Figure 10: Gate drive loop comparison of a standard three-terminal package (left) and a four-terminal package with Kelvin source (right)](image)

It’s important to mention that Kelvin source packages solve the $L_{Sc}$ negative effect on the gate drive and switching speed. However, the $L_{Sc}$ will still add to the total loop inductance, which is a crucial parameter that causes ringing in fast-switching applications such as server SMPS with wide-bandgap (WBG) switches. For that reason, the package $L_{Sc}$ is preferably the lowest even when using a Kelvin source. More details are available in the referenced application note.

**SUMMARY**

This article discussed the significance of power semiconductor packages in meeting the power and density requirements of server power supplies, specifically for silicon and WBG switches.

A quick introduction to server SMPS applications and trends was presented, followed by a discussion on SMD packages regarding assembly implementations, thermal performance, and low-inductance parasitic advantages in a high-frequency operation.

Table 1 summarizes Infineon’s SMD package portfolio used in server SMPS, comparing their main parameters.
To learn more about Infineon's design solutions for SMPS that meet the increasingly high demands of servers and data centers, please click here. Also, discover our full spectrum of innovative power technologies (Si, SiC, and GaN). For high-voltage power MOSFETs, click here. For WBG solutions, click here.

References


Design Notes on High-Voltage Power Device Package

By Stefano Lovati, technical writer for EEWeb

Renewable-energy applications, as well as all kinds of energy-efficiency technologies, require reliable, compact, and thermal-efficient power devices. For driving innovation in wind turbines, smart grids, solar power systems, solar photovoltaics, and electric-drive vehicles, devices with high power density, high switching frequency, and the ability to operate at extreme temperatures and voltages are required. Demanding power applications impose challenges involving not only the device itself but the package surrounding it.

Even though silicon has long dominated power applications, demand for increased efficiency and power density, as well as enhanced performance and reduced costs, have prompted a paradigm change in power electronics toward wide-bandgap semiconductors like silicon carbide and gallium nitride. Despite the fact that wide-bandgap devices have begun to enter the commercial market...
in recent years, their package designs have not yet matured, particularly for high-temperature and high-voltage applications. In this article, a 5-kV double-sided cooled GaN power module built for this purpose (as part of a study funded by the Advanced Research Projects Agency–Energy) will be presented. Read the original article here.

PACKAGE DESIGN

The design of the GaN power module is shown in Figure 1. It includes four GaN devices bonded to molybdenum posts at the top and bottom of the package. The posts' outer ends are bonded to a direct-bonded copper (DBC) substrate with ceramic substance alumina (Al₂O₃). Although baseplates are attached to the outer faces of the DBC substrates in this package design, the material stackup can also be terminated at the DBC layer. In some circumstances, having a baseplate is advantageous, as it allows for more heat distribution within the package, increasing the thermal management solution's effectiveness.

THERMAL ANALYSIS

The thermal simulations aimed to determine the best method of cooling the device within the design constraints, as well as to evaluate the effectiveness of the proposed cooling technology. Finite-element analysis was used to evaluate two cooling techniques, as shown in Figure 2. The heat-exchanger method (Figure 2, top) is similar to traditional coldplate cooling, with heat exchangers on both sides of the package. A convective-heat–transfer coefficient is used to represent the heat exchanger (h).

Due to the long conduction paths, the 5-kV design necessitates physical separation of the terminals and the package being filled with a dielectric fluid for electrical insulation. As a result, heat removal from the package using traditional methods (Figure 2, top) becomes more challenging. The alternative solution (Figure 2, bottom) tries to turn this disadvantage into a cooling benefit by using dielectric fluid as a coolant and long electrical standoffs or posts as fins, effectively turning the package into a heat exchanger.

The convective-heat–transfer coefficient was swept across a range of values from 10 W/m²K, which represents natural convection in air, to 100,000 W/m²K, which represents a very aggressive single-phase liquid-based heat exchanger or phase-change heat transfer, to evaluate and
compare the two cooling methods. The oil flow-through design performed better than the heat-exchanger design. Moreover, it is a promising technique for applications in which water-based coolants near the devices are not available. However, to work effectively, it would require additional surface enhancement (such as fins) to be added to the posts, which, in turn, would require additional design and evaluation on the electrical design to ensure that the surface enhancements would not result in unwanted electrical discharge. Additional design work would also be required to optimize the fluid flow through the package.

The temperature was plotted along a line through the middle of the device to detect thermally problematic spots within the package (Points 1 to 2 in Figure 3). High-temperature gradient locations (horizontal lines in the plot) denote highly thermally resistive components, whereas low-temperature gradient locations (vertical lines) denote highly thermally conductive components. The DBC substrate and the thermal interface material have the highest thermal resistance per length in the package.

To fully exploit the double-sided cooling, three alternative designs were evaluated: all of the devices on one DBC and two versions of splitting the devices between the two DBCs. Figure 4 shows the target heat flux of 300 W/cm², as well as a baseline (devices in the middle) for comparison. If the package utilizes just one DBC, the heat-exchanger performance requirement for the target heat flux is reduced to 3,100 W/m²K, or 2,200 W/m²K if the package uses heat exchangers on both sides. The heat-exchanger performance required for dividing the devices evenly across the two DBCs (inline or diagonal layout, depicted in Figure 4) is reduced to 1,400 W/m²K.
The performance of an off-the-shelf heat exchanger was quantified using computational fluid dynamics, and it was discovered that the heat exchanger could be employed on double-sided cooling layouts but not single-sided cooling layouts or layouts with devices in the center.

**THERMOMECHANICAL ANALYSIS**

The goal of the thermomechanical simulations was to look at the reliability of a few package designs, notably the diagonal, inline, and baseline configurations, as shown in Figure 4. Under a thermal-cycle–loading condition, strain-energy–density values in the various attachment layers within these package designs were computed and compared. The load was applied to a thermal cycle from –40˚C to 200˚C with a 5˚C/minute ramp rate and a 10-minute dwell at both extreme temperatures, and strain-energy-density-per-cycle data was obtained at the different attachment layers.

![Figure 4: Comparison of three alternative designs](image)

Figure 5 shows the strain-energy–density values of several layers in the baseline, diagonal, and inline package designs. The obtained results suggest that the post attach is the most susceptible to heat-cycle degradation, followed by the diagonal and inline configurations.

![Figure 5: Strain energy density for different package configurations](image)
by the device attach and device post-attach. In addition, there was no discernible difference in the thermomechanical performance of the attachment layers across the various package design configurations.

The next stage in this research will be to see how the length of molybdenum posts affects the package’s thermal performance and reliability, as well as to increase the number of devices to improve the voltage rating.

References


POWERUP PROCEEDINGS

Agenda

Speakers
Gallium nitride has become the de facto material in third-generation semiconductors. However, making GaN wafers in the quality you need and the thermal resistance you desire are challenges that fabs are still trying to overcome.

The mismatch of lattice constant and thermal expansion coefficient between GaN epi layers and substrates such as silicon, sapphire, and silicon carbide lead to the dislocation and cracking of epi layers.

A common method for thermal management is using substrates with high thermal conductivity, such as SiC or diamond, as the heatsink. However, both the lattice mismatch and the coefficient of thermal expansion mismatch between GaN and SiC/diamond make the heteroepitaxy very challenging. Furthermore, the conventional nucleation layer exhibits low thermal conductivity due
Semiconductors

to the defects and poor crystallinity. The thick buffer with low thermal conductivity adds significant thermal resistance to the heat dissipation path from the device to the substrate, as most of the heat is generated within the active layer at the top. Defect and boundary scatterings within the transition layer, at the interface between the substrate and transition layer, and by near-interfacial disorder contribute together to large thermal resistance.

Though there are choices of substrates that can be used for growing GaN epi, some are not foundry-friendly, whereby CMOS processes are used. Another reason is that the lithography tools and other tools for making CMOS devices that are state of the art are available only on larger-scale wafers. Hence, GaN-on-Si with wafer sizes of up to 12 inches has advantages. GaN-on-sapphire at 6 inches is relatively inexpensive; however, many foundries do not accept sapphire, and its thermal conductivity is poor.

To grow high-quality GaN, expensive substrates such as bulk GaN and SiC are required. Therefore, the production cost for the device manufacturing is significantly higher than Si-based electronics. To achieve cost-effective state-of-the-art GaN power device performance while efficiently managing the generated heat, the epi layer could be removed from the substrate, enabling substrate reuse, and directly bonded to a heatsink to improve device thermal performance. However, existing removal processes such as those involving photoelectrochemical etching, mechanical spalling, and laser interface decomposition suffer from slow processing speed and/or significant surface roughening/cracking, limiting the process yield and practicality of substrate reuse. Therefore, the process cost of these conventional methods typically exceeds GaN substrate cost, limiting manufacturing.

When the device needs better quality, in terms of dislocation density, thermal properties, and higher frequencies that are needed for high-voltage devices in power for automotive, RF, and data-center applications, GaN-on-SiC tends to be the way to go. However, GaN-on-SiC is an expensive solution. Once the good-quality GaN epi layer is grown on the SiC substrate, you will get a better GaN device for power and RF applications. The drawback is that SiC substrates are very expensive. The SiC substrate is no longer needed after the GaN epi layer is grown on top of it.

To summarize:

▶ Large GaN wafers of current technology have higher dislocation density (poor crystallinity).

▶ GaN-on-Si wafers tend to use very thick buffers and interlayers to manage the stress, making it difficult to manage thermal conductivity.

▶ Most other substrates are very expensive, and scaling to larger wafers is not an option.
WHAT NEW TECHNOLOGIES CAN HELP SOLVE THESE PROBLEMS?

Until now, there has been no easy way to remove the SiC or Si substrate from this device structure, and hence, the device was very expensive.

The invention of remote epitaxy and 2D material-based layer transfer (2DLT) technology at MIT made it possible to grow the compound materials through the 2D material. Once grown, it can be lifted off to release the substrate from it and reuse.

With this technology, one can create the GaN epi layer and lift it off from the expensive SiC substrate and transfer it onto a low-cost substrate. This will free up the SiC substrate to be reused in the next GaN epi wafer growth (see Figure 1).

The advantages of remote epitaxy and 2DLT solutions are instantaneous liftoff of the GaN thin film without any polishing or other post-processing step. No polycrystalline or amorphous regions will be introduced by the bonding or exfoliation process. No nucleation layer with poor crystallinity is required, so it is possible to obtain ultrathin (<200 nm) GaN freestanding membranes. This is not possible with any other existing technology.

The new age of GaN has started. Remote epitaxy and 2DLT are enabling the technology to scale the GaN to a larger size, improve the quality by reducing the dislocation density, and help manage thermal properties at low costs.

Reference
Integrated Circuit GaN Inverter for Motor Drive Applications Above 1 kW

Leading the evolution of GaN technology, EPC introduced in 2019 the first IC of the ePower family. These devices follow the “digital in, power out” concept to simplify converter and inverter designs. The experimental results of six EPC23101 ICs connected in inverter topology to drive a motor are presented in this article.

By Marco Palma, director of motor drive systems and applications at Efficient Power Conversion (EPC)

Since its introduction, gallium nitride technology has opened a new era in the world of power electronics. The three most important parameters for GaN technology are the higher bandgap,
critical field, and electron mobility. When these parameters are combined, because the critical field of the GaN crystal is 10× higher, it follows that the electrical terminals can be 10× closer together when compared with a silicon MOSFET. This leads to a clear differentiation factor between GaN and silicon: Medium-voltage GaN devices can be built on a planar technology, while this is cost-prohibitive for silicon devices. To be competitive, silicon devices are made on a vertical technology, making it physically impossible to have two power devices in the same chip. EPC’s GaN-on-Si planar technology does not have this limit of having to be built vertically, and a schematic cross-section of an integrated circuit that takes advantage of this is shown in Figure 1.

![Figure 1: EPC GaN technology enables integration of power devices with gate driver logic](image)

**GaN IC POWER STAGE CHIPSET — EPC23101 IN COMBINATION WITH EPC2302**

Starting with discrete lateral eGaN FET devices, EPC quickly moved to higher levels of integration. In 2019, the ePower Stage IC family of products redefined power conversion by integrating all requisite power system-on-a-chip functions in a single GaN-on-Si IC at higher voltages and higher frequency levels — beyond the reach of silicon. Most recently, in 2021, the EPC23101 in combination with the EPC2302 power stage chipset was introduced to the market (Figure 2).

The EPC23101 is a 100-V–rated monolithic component that integrates input logic interface, level shifting, bootstrap charging, and gate drive buffer circuits, along with a high-side, 2.6-mΩ typical $R_{DS(ON)}$ GaN output FET. The EPC23101 IC requires only an external 5-V ($V_{DRV}$) power supply. Internal low-side and high-side power supplies, $V_{DD}$ and $V_{BOOT}$, are generated from the external supply via a series-connected switch and a synchronous bootstrap switch. The internal circuits can be disabled to reduce quiescent power consumption by connecting the EN pin to $V_{DRV}$.

**EPC9173 MOTOR DRIVE REFERENCE DESIGN WITH EPC23101**

To demonstrate the capabilities of the EPC23101 IC in a motor drive inverter, EPC released the EPC9173 reference design. On this board, each half-bridge of the three-phase inverter comprises two EPC23101 ICs with their PWM signals cross-connected, allowing the insertion of a source shunt to read the current.
as shown in Figure 3, with a portion of the schematic.

By using the same IC for the low-side switch, it is possible to have a balanced half-bridge inverter, and both switches can float with respect to the power ground. This makes the insertion of the source shunt easier, avoiding ground bouncing on the input PWM signal nodes. The EPC9173 board includes an overcurrent detection circuit that can be used either as an overcurrent or as a current-limit function, depending on the desired algorithm and modulation.
APPLICATIONS

PWM frequency increase and dead-time reduction

GaN ICs and FETs bring several advantages in motor drive applications. The easiest advantage to understand is the reduction of inverter size, which is due to an intrinsic smaller dimension of a GaN FET and ICs versus the equivalent MOSFET. However, to get the most out of the new technology, it is better to operate a motor at a higher PWM frequency and to consequently reduce the dead time.\(^2\)

Increasing switching frequency helps to reduce the input filter and to remove the need for electrolytic capacitors. A comparison between two inverters — one running at 20-kHz, 500-ns dead time and the other, based on GaN, running at 100-kHz, 14-ns dead time — is shown in Table 1. With the GaN inverter, the motor is more efficient because many energy-wasting harmonics are removed.

Applications with low L/R time constant in the motor

All applications that require high electrical frequency and fast dynamics, such as drone propellers and e-bike in-pedal motors, use very low-inductance (single-digit–microhenry range) motors. With the advent of more efficient magnetic circuit designs realized by better materials and higher-strength permanent magnets, the number of turns on an electromagnetic phase can be reduced and still produce the same back EMF.

The current rise with time is related to the ratio of voltage to inductance, and as inductance decreases, the current rises quicker, as does the PWM induced current ripple. The decreased current rise time and larger ripple increases the amount of heat generated and creates additional EMI noise, which is not desirable. In general, these motors have a small time constant, \(t = L/R\), that can benefit from a 100-kHz PWM frequency.

Input current and voltage ripple

The input voltage ripple \(\Delta V_{in}\) in an inverter is proportional to the output phase current and inversely proportional to the PWM frequency and input capacitance, as per the following equation:

\[
\Delta V_{in} \propto \frac{1}{f_{PWM}} \frac{I_{phase}}{C_{in}}
\]

The desired \(\Delta V_{in}\) ripple depends on the EMI constraint given by the emissions generated by the cables from the DC source to the inverter. If the PWM frequency is in the range of 20 kHz, the required input capacitance (\(C_{in}\)) can only be practically obtained by using electrolytic capacitors that are bulky.
and less reliable than ceramic capacitors. Moreover, the electrolytic capacitors are limited by the RMS current that can flow through them. When the frequency is increased to 100 kHz, designers can use ceramic capacitors such as X7R. The EPC9173 reference design provides for both electrolytic and ceramic capacitors, giving designers a chance to select their preferred switching frequency and to add or remove the capacitors as preferred.

**Power tools with trapezoidal modulation**

Many power-tool applications are still using trapezoidal-modulation schemes and related inverter schematics. With the current-limiting cycle-by-cycle scheme and low-inductance motors, the lower the PWM frequency, the higher the current ripple. This in turn generates heat and unnecessary power dissipation. Using a GaN inverter with the same trapezoidal scheme makes it possible to increase the PWM frequency and then reduce the current ripple, obtaining higher efficiency, less heat, and fewer vibrations.

**CONCLUSION**

When dealing with motor applications, GaN inverters can increase the efficiency of the system if PWM frequency is increased, the dead time is drastically reduced, and the input capacitance is converted from electrolytic capacitors to ceramic capacitors. Using EPC’s new GaN ICs, such as EPC2152 and EPC23101, results in increased power density and system efficiency while saving much system design effort.

**References**


Sun to Wheels: Powering a Renewable Future with Silicon Carbide

By Guy Moxey, senior director for power products at Wolfspeed

As the world advances toward a sustainable, greener future, many countries are powering down fossil-fuel energy generation in favor of renewables. The global weighted-average cost of electricity from new utility-scale solar photovoltaic (PV) projects fell by 85% between 2010 and 2020, onshore wind by 56%, and offshore wind by 48%. Renewables have thus become the typical route for energy capacity addition in nearly all countries, and the compound annual growth rate of cumulative PV installations, including off-grid, reached 34% between 2010 and 2020.¹

This growth is set to continue with the added thrust toward increasing energy efficiency. An International Renewable Energy Agency (IRENA) report asserts that limiting global warming to 1.5°C would require cutting 36.9 gigatons of annual CO₂ emissions and has recommended a target of an additional 444 GW/year of solar PV and 248 GW/year of wind energy until the year 2050. IRENA estimates that significant increases in renewable energy and energy efficiency can each contribute no less than 25% toward achieving the targeted emissions reduction, while another 20% can be reached through electrification of such applications as transport.²
While research in new wind turbine designs and perovskite-based solar cells is pushing the limits of energy conversion efficiency, the power semiconductor chain between the generation to application of renewable energy need no longer be the weak link from the sun to the wheels. There are immense size, weight, power, and cost benefits available today from simply swapping out legacy semiconductor technology for silicon carbide in energy connection, distribution, and storage systems.

HIGH EFFICIENCY IN POWER ELECTRONICS CHAIN

For both 5- to 15-kW residential single-phase and 30- to 100-kW commercial three-phase architectures, arrays of solar panels are used to increase the voltage and reduce I^2R losses in connections and cables. The PV array voltage is typically boosted to a regulated DC that charges an energy storage system (ESS) that helps tide over the power fluctuations typical of solar energy generation. Regulated DC is supplied to an inverter for DC/AC conversion, while a maximum-power point-tracking (MPPT) controller optimizes the load on the panels for the highest energy efficiency.

Wolfspeed offers SiC devices that suit each stage in this power electronics chain and at the power levels needed by applications ranging from residential to light commercial to utility-scale. The company’s technology helps designers achieve higher system-level efficiency and power density with lower system cost — all main driving factors in the renewable energy market (Figure 1).

DC/DC boost

The DC/DC section is used to boost the variable PV panel voltages. By replacing silicon diodes and MOSFETs in this section for string-type inverters with Wolfspeed’s SiC modules, designers can reduce system size by 70% and increase system efficiency by 1% while lowering overall cost by 30%. This is the direct result of the ability to use higher switching frequencies, which reduce inductor, capacitor, filter, and transformer sizes, costs, and packaging.

Energy storage systems

The ESS application offers tremendous opportunity for SiC implementation from residential through industrial applications by fulfilling system requirement gaps left by silicon in DC/DC boost/MPPT, bidirectional active front ends, and DC battery chargers.

Wolfspeed tests with its SiC solutions have shown a nearly 3% increase in system efficiency, up to 50% higher power density, and significant reductions in passive component volume and passive BOM costs.

Mid- to high-voltage (MV/HV) SiC MOSFET modules from 3.3 kV to 20+ kV open up several existing and emerging application spaces, including grid-tied inverters, superchargers, and traction.

Grid-tied PV inverters

Enabled by MV/HV SiC devices, these inverters can connect solar farms directly to the grid, thereby eliminating heavy, expensive, and lossy transformers from the power electronics chain. This lowers
installation, operating, and site costs of the PV power system.

For instance, such a 2-MVA grid-tied inverter system would comprise the Wolfspeed 1,700-V SiC half-bridge modules operating at 40 kHz, a smaller medium-frequency transformer at 40 kHz, and Wolfspeed 10-kV SiC modules at 10 kHz. It would weigh less than 1,000 pounds, excluding the transformer, and achieve over 98% CEC efficiency.

**DC fast charging**

Traditional fast chargers typically use low-frequency transformers that add several thousand pounds to the overall system weight. This type of 500-kVA system would be a 5,190-liter, 3,537-kg charger with >28-kW power losses.

A modern 500-kVA fast charger based on Wolfspeed’s 6.5-kV SiC and a >20-kHz solid-state transformer is a £1,298-liter, £530-kg system with £11.25-kW power losses. The SiC-based DC fast charger can therefore achieve full charge in less than four minutes, with a system that is >75% smaller and >85% lighter and has >60% lower losses as well as >40% lower costs.

**Traction and mobility**

MV/HV SiC modules can decrease annual fuel consumption of transport by 1% to 4% and, in drive systems of heavy equipment, result in substantial savings on drive systems, cooling, and wiring.
Wolfspeed offers SiC discrete devices and modules that cover the industry’s widest application power scale (Figure 2). The company’s MV/HV solutions, rated from 3.3-kV LM3 modules to 6.5-kV MM3 and 10-kV XHV-9 modules, address a broad range of voltage, current, and isolation requirements from the applications discussed above.

Figure 2: Wolfspeed’s SiC portfolio offers renewable energy applications the power scalability from less than 2 kW into the megawatt range

As a vertically integrated SiC supplier with the largest market share and growing, Wolfspeed has over 30 years of experience and millions of MOSFETs and diodes in the field operating for trillions of hours.

To talk to an expert about the benefits of SiC technology and the devices that best suit your application, contact Wolfspeed.

References

System Benefits of GaN and SiC Devices in the Next Generation of On-Board Chargers and USB-C Adapters with Ultra-High Power Density

By Matthias J. Kasper, principal engineer; Jon Azurza, senior staff engineer; and Gerald Deboy, distinguished engineer for Power Discretes and System Engineering, all at Infineon Technologies

The adoption of wide-bandgap (WBG) power devices such as silicon carbide MOSFETs and gallium nitride HEMTs is now in full progress across a wide range of market segments. In many cases, WBG power devices are replacing their silicon counterparts and enable higher efficiencies in existing systems. In other cases, such as the totem-pole configuration, WBG power devices enable a simple option for bridgeless power-factor correction (PFC) with continuous-conduction modulation.

In this article, we will outline how we derive optimal use cases for GaN and SiC power devices in a holistic system optimization approach.

DEVICE TECHNOLOGY

Infineon Technologies offers the whole spectrum of power semiconductor technologies ranging from its established Si superjunction devices to SiC MOSFETs and GaN e-mode HEMTs. The company's SiC
MOSFETs (see Figure 1a) feature a unique asymmetric trench structure, where the channel mobility is optimized by aligning the channel to the a-plane of the SiC crystal. Furthermore, a large portion of the trench is embedded into a p+ region, which extends below the bottom of the trench and thus reduces the off-state critical field and acts as a body diode. As a result, with Infineon’s trench design compared with planar DMOS concepts, high levels of gate oxide robustness can be reached by allowing lower gate drive voltage for similar $R_{DS(on)}$ performance.

The basis for analyzing the value proposition of our CoolGaN devices (see Figure 1b) is Infineon’s proprietary gate injection transistor (GIT) technology. This concept has the advantage of separate optimization of on-state resistance and current capability versus threshold voltage, which can increase the threshold voltage without affecting the $R_{DS(on)}$ value. Another advantage is the self-clamping property of the p-GaN gate structure, which acts as a diode and increases the robustness in case of overvoltage spikes on the gate. Another technology-specific advantage is the hybrid drain structure, which injects holes from the drain in hard-switching events and helps to eliminate detrimental effects from residual charges such as dynamic $R_{DS(on)}$ and current collapse.

**Figure 1: Wide-bandgap semiconductor technologies: (a) CoolSiC (b) CoolGaN GIT HEMT**

**WIDE-OUTPUT VOLTAGE RANGE 240-W USB-C CHARGERS**

With the goal of designing the next generation of chargers, an ultra-compact charger supporting two USB-C output ports with 5 A each with an output voltage range of 5–48 V is envisioned. The charger needs to work at universal input AC lines ranging from 90 V to 264 V. Specifically, these wide input and output voltage ranges with two individual ports call for a three-stage approach consisting of a totem-pole PFC stage with two interleaved high-frequency bridge legs, a DCX stage (“DC transformer”) running continuously at its resonance frequency, and two subsequent buck stages. The PFC stage and the DC/DC converter switch at 400 kHz (800-kHz effective frequency with two legs) and 425 kHz, correspondingly. The system employs integrated power stages with CoolGaN GIT HEMTs in half-bridge configuration and matching drivers in all high-voltage sockets and CoolGaN Schottky gate HEMTs as 100-V devices. The entire system achieves an outstanding power density of 42 W/in.² (uncased).

Figure 2 shows the topology and hardware demonstrator.
NEXT GENERATIONS OF ON-BOARD CHARGER SYSTEMS WITH SiC AND GaN DEVICES

The current generation of on-board chargers with Si devices achieves about 2 kW/l with phase-modular approaches consisting of three separate PFC stages and three subsequent DC/DC stages. Replacing the high-frequency semiconductor devices with SiC MOSFETs increases the power density to levels of about 4 kW/l. To increase the power density beyond these values, a true three-phase system design has to be considered.

The key enablers for the highest power densities can be seen in the ultra-compact 10-kW EV charging unit shown in Figure 3, which can serve as a blueprint for next-generation on-board chargers. This three-phase EV charging system supports a very wide range of output voltages of 250 V to 1,000 V. It consists of a Vienna rectifier PFC stage and four interleaved dual active bridges (DAB) for the isolated energy transfer to the battery. Both PFC front-end and DC/DC stages are compatible with 600-V power devices due to the three-level nature of the Vienna rectifier and the stacked approach for the DC/DC stages.

For operating the Vienna rectifier at switching frequencies beyond 500 kHz, the switching losses have to be reduced. Hence, we apply a new “synergetic control” strategy, wherein the DC-link voltage follows the six-pulse shape of the rectified three-phase input voltage. This control scheme enables a reduction of switching losses of up to 86%. Instead of switching all bridge legs simultaneously, only the leg carrying the lowest current is switching. Using this technique, an increase of switching frequency to 550 kHz has been achieved. Discrete CoolGaN GIT HEMTs with 70-mΩ $R_{DS(on)}$ are used.
in the Vienna rectifier front end, while devices with 42-mΩ $R_{\text{DS(on)}}$ are employed in the DAB stages.

The DAB stages run between 140 and 400 kHz and achieve zero-voltage switching in most of their operation points.

The entire system achieves a power density of 10 kW/l or 163 W/in.³, respectively, at a peak efficiency of above 95%.

![Diagram of the EV charging unit](image)

**Figure 3: 10-kW EV charging unit supporting a wide output voltage range and a power density of 10 kW/l (163 W/in.³)**

(Note: The authors would like to thank Professor Johann Kolar, Yunni Li, and Michael Haider from the Power Electronic Systems Laboratory at ETH Zurich for their ongoing cooperation on the EV charging unit).

Reference

- **PowerUP Expo 2022**
Non-CMOS-Compatible SiC Power Device Fabrication in Volume Si Fabs

Adapted from a presentation by Victor Veliadis, executive director and CTO of PowerAmerica and professor of electrical and computer engineering at North Carolina State University

Silicon carbide devices are displacing their incumbent silicon counterparts in several high-volume power applications. As SiC market share continues to grow, the industry is lifting the last barriers to mass commercialization that include higher-than-Si-device cost, relative lack of wafer planarity, the presence of basal plane dislocations, reliability and ruggedness concerns, and the need for a workforce skilled in SiC power technology to keep up with the rising demand. To enable cost-effective SiC manufacturing, high-yielding fabrication processes are required. In my PowerUP presentation, I will summarize key aspects of SiC fabrication technology and outline non-CMOS-compatible processes that have been streamlined to allow for mass SiC device fabrication in conventional mature Si fabs.

SiC WAFERS

Today, the SiC wafer represents 55% to 70% of the overall SiC device cost, a consequence of its uniquely complex fabrication specifics. Conventional SiC substrates are primarily grown by the seeded sublimation technique at temperatures of ~2,500°C, which creates process control challenges. Crystal
expansion is limited, requiring the use of large, high-material–quality seeds, and the sublimation growth rates can be relatively low, in the order of 0.5–2 mm/h. Dislocations propagate through the boule and are present in the device wafers. Furthermore, SiC material’s hardness, which is comparable to that of diamond, makes sawing and polishing SiC substrates slow and costly relative to Si.

The epitaxial layers, where SiC devices are fabricated, are grown by chemical vapor deposition in horizontal or planetary reactors at 1,500°C to 1,650°C. Pressure typically ranges from 30 to 90 Torr, and growth rates can be as high as 46 mm/h. Epitaxial growth is done on 4° off-cut substrates to maintain the polytype stability of the substrate. Epitaxy goals are to minimize defect generation, to restrict “performance degrading” defect propagation from the substrate into the epitaxy, and to ensure that performance-degrading defects propagating from the substrate into the epitaxy transform into benign defects. As defects in SiC wafers limit large-area device yields, and numerous devices are paralleled in modules to increase current output, tight epitaxial doping and thickness uniformities are highly desirable, particularly as wafer size increases.

Overall, SiC wafer synthesis is more complex and slower than that of silicon. The result is more expensive wafers and, ultimately, higher device costs. A key part of the vertical integration occurring in today’s SiC industry is securing internal substrate and epitaxy wafer capabilities to eliminate purchasing profit margins. In addition, opportunities for disruptive SiC substrate formation, boule slicing, sawing/polishing, etc., have a high return and are being sought by several companies.

**SiC DEVICE FABRICATION**

Numerous well-established processes from silicon technology have been successfully transferred to SiC. However, SiC material properties necessitate optimization of specific processes, including wafer thinning, etching, heated implantation and anneal, and low-resistivity ohmic contact formation. SiC is inert against chemical solvents, and only dry etching is practical. Furthermore, the hardness of SiC results in low photoresist selectivity, and “hard” masks, usually composed of metals or dielectrics, are required for SiC photolithographic patterning and etch.

Conventional thermal diffusion is not realistic in doping SiC due to its high melting point and the low diffusion constant of dopants within SiC. Heated ion-implantation is typically performed for doping densities of $10^{16}$–$10^{20}$ cm$^{-3}$ (the higher doping densities assisting with ohmic contact formation), and room temperature implantation can work well for low implant doses ($\sim 10^{15}$ cm$^{-3}$). Nitrogen/phosphorus and aluminum are the preferred impurities for n-type and p-type SiC doping, respectively. After ion implantation, a 1,600°C to 1,800°C anneal is performed for lattice damage recovery and high dopant electrical activation. The as-implanted depth profiles are retained after the anneal for Al, P, and N, as expected from their low diffusion constants. The lack of diffusion makes it easy to form shallow junctions and difficult to form deep ones in SiC. During the anneal, a protective cap layer covering the SiC wafer protects its surface from degradation due to Si desorption and migration of surface atoms (Figure 1).
The high value of the SiC/metal barrier results in rectifying metal contacts, and post-metal–deposition anneal is required for ohmic contact formation. Typically, a 50- to 100-nm Ni layer is blanket-deposited and patterned on the wafer for the simultaneous ohmic contact formation on the n-type and p-type doped regions. High temperature annealing of the Ni-patterned wafer creates Ni-silicide for low-resistivity ohmic contact formation.

Unlike Si wafers, SiC wafers are transparent. This complicates the use of “silicon” tools for CD-SEM and metrology measurements, as the focal plane is determined with the use of an optical microscope. SiC-specific wavelength metrology/inspection tools are now available from multiple vendors.

Another issue is the relative lack of flatness of SiC wafers, compared with those of Si, which can complicate photolithography. In addition, the high-temperature SiC processing can further degrade wafer flatness, occasionally rendering wafers unusable. This is particularly problematic with the thick epitaxy wafers used in 3.3-kV device fabrication. Efforts are underway to produce flatter-starting SiC wafers and to minimize flatness degradation during fabrication.

Lastly, the poor SiC/SiO₂ interface quality reduces inversion layer mobility. Thus, passivation techniques, including annealing in nitrides, are utilized to improve the SiC/SiO₂ interface quality similar to the case of silicon.

**SiC Fab Infrastructure**

Device manufacturers have developed IP for several SiC processing steps and compete on both design and processing. Although SiC is not fully CMOS-compatible, the SiC industry has leveraged Si technology processes and infrastructure by making the relatively small financial investments required to adapt existing fabs. Today, SiC manufacturing is mature, and its fab infrastructure mirrors that of Si. Integrated SiC device manufacturers coexist with foundries and fabless companies, and design houses provide expertise and IP that can be leveraged to accelerate entry to market (Figure 2).

SiC device fabrication in volume fabs alongside Si has emerged as a cost-reduction model exploiting
silicon manufacturing economies of scale. Through repurposing older, fully depreciated 150-mm (and soon 200-mm) Si fabs, SiC power devices can be manufactured with the relatively small investments necessary to support the unique SiC processing steps. Minimizing fabrication cost by exploiting the mature Si volume production assumes the fab is loaded close to capacity with standard Si and SiC processes running on the same lines.

In addition, aggregating the demand for SiC substrates and epilayers in volume fabs contributes to lower material costs. Lower fabrication costs in a fully depreciated Si + SiC “capacity loaded” fab, coupled with decreased material costs, can lead to significant price reductions for SiC devices. This approach offers a new opportunity for outdated Si fabs, which have not kept up with the channel-length reductions of the last two decades, to continue manufacturing legacy Si parts while ramping up SiC fabrication that requires relatively modest ~0.3-µ design rules.

SUMMARY
The compelling efficiency and system benefits of SiC are leading to wide adoption that enables manufacturing economies of scale and lower system costs. The wafer represents a disproportionately high percentage of the overall SiC device cost compared with that of Si. SiC manufacturing is mature, including non-CMOS-compatible processes.

Reference

▶ PowerUP Virtual Conference (June 28–30, 2022)
Consider how many man-made disasters we’ve had to cope with in the last 50 years — Chernobyl is one of them. Now we’re dealing with a potentially more serious issue: climate change. The pace with which climate change is unfolding makes it more hazardous and devious than any previous disaster. Its consequences have been felt for decades, despite many academics having used predictive models to anticipate them. Its consequences are intensifying, speeding up, and eroding the foundation of our ecology. Now is the moment to act: If we do nothing, extreme weather will become the norm, wreaking havoc on our ecosystem and resulting in the extinction of entire species. Not only that, but a rise in sea levels will lead to population displacement, resulting in political instability.

Hassane El-Khoury, president and CEO of onsemi, noted in his opening during the PowerUP Expo the scientific aspects that demonstrate with data how evolution is increasingly worrying and important decisions that need to be made.
“Our responsibility as a technical community and as innovative engineers is to take action to do something,” said El-Khoury. “Oil, natural gas, and coal have been the largest contributors to CO₂ emissions, making up about 83% of the global emissions problem. That is billions of metric tons emitted by these markets alone. But suppose you analyze the carbon footprint that these industries contribute to our environment. In that case, you find that if we maintain and do nothing, the budget — that is, this 1.5°C that we all believe is the threshold to maintain — will be exceeded by 2030. And if you think 2030 is too far away, it is eight years from now — not even a design cycle for a car that we are familiar with. So in 2030, the actions we take today and the projects we are working on today are the projects that will help us maintain our competitiveness.”

Figure 1: The path to decarbonization requires us to transform energy sources and land-use systems from 2020 to 2050. (Source: onsemi and McKinsey)

Figure 2: Focusing on the shift in mobility from 2020 to 2050 (Source: onsemi and McKinsey)
THE FUTURE OF ENERGY

“We are the solution,” said El-Khoury. “How can we implement this solution to serve the common good we focus on? We have a responsibility not only individually but also organizationally and of the companies we work for, in our home and in our personal lives, in the way we consume, and in the way we are responsible for the energy provided to us.”

Industry areas such as energy, mobility, and manufacturing are important to environmental success. Disruptions in various areas are required to decrease, control, and manage the emissions problem. We must expand our reliance on renewable energy and lower our dependency on oil, gas, and coal. “Not just because it is the ethical thing to do, but also because renewable energy is abundant and has no negative environmental impact,” said El-Khoury. “However, it is a step in the right direction in terms of CO₂ reduction.”

The introduction of electric cars will aid in the reduction of emissions, but the infrastructure from which the energy is obtained, as well as the entire process of creating electric vehicles, must be considered in terms of environmental effect. The lack of a widespread charging infrastructure will stymie electric-car adoption. The grid will be unable to handle the massive charging network of EVs if we do not create renewable energy.

Using energy generated from renewable sources from the grid itself to distribute it is the way to reduce this dependence. And from a charging perspective, focusing on high-power charging, which reduces the time to charge an EV to less than 30 minutes, will promote the adoption of EVs and consequently reduce the dependence on internal combustion engines.

“We need to accelerate the pace by enabling all of these technologies surrounding EVs to minimize so-called range anxiety,” El-Khoury said.

According to El-Khoury, all of these factors may be linked back to two routes. The first is to reduce energy consumption through energy-efficiency architecture and platforms, and the second is to change the energy sources that power these highly efficient platforms. “As a result, we must minimize consumption and shift our energy source,” he said. “And it will only be when we do both that we will begin to make headway toward a brighter future.”

This, according to El-Khoury, is a sustainable ecology. And a healthy ecosystem is a circle with interconnections, starting with renewable energy (which includes storage) and progressing through smart factories and automation, cloud-based energy (which powers all content and intelligence in the cloud), and mobility with EVs (which includes advanced security) to promote efficiency in vehicle electrification, charging, EV deployment, and infrastructure. “You only have a healthy environment when you create a balance between all of these components,” El-Khoury said.
From a 5G energy and cloud perspective, we need to accelerate the pace of data center deployment, reducing the energy requirements that cannot increase proportionally to the complexity of a data center. The complexity of data centers is bound to increase over the years. Scaling energy, therefore, at a much more efficient pace is an important path. “Our focus is on providing high-efficiency smart power solutions to reduce consumption, through intelligence and efficiency, and thus enable our customers to have an impact on emissions — and these are drastic impacts,” said El-Khoury.

“We cannot be blind to the fact that as producers of all these great technologies that enable this mission, we are not responsible for how we create them. We have to address the sustainability needs of today and the future. We must lead and manage our operations in a way that is responsible through abatement and conversion. To achieve our mission, we will be carbon-neutral by 2040. Only then will we feel proud to provide smart solutions that enable everyone to meet not only their own demand but also that of their customers — that is, all of us who are consumers of these technologies.”

Reference

▶ PowerUP Virtual Conference (June 28–30, 2022)
The Rise of Wireless Power Networks

By Cesar Johnston, CEO of Energous

Soon, internet-connected devices will outnumber all of Earth’s humans by a ratio of 5:1.

That’s according to analyst firm IDC, which projects a 3x increase in the global IoT ecosystem between now and 2025, when the number of internet-of-things devices is expected to reach 39.3 billion, up from about 12 billion devices today.

This exceptional growth brings with it both tremendous potential for positive outcomes from IoT deployments as well as concerns around how to reliably power these billions of devices that are often located in rugged, hard-to-reach environments and/or away from central power sources.

This challenge stems from one basic fact: Most of the 12 billion–plus IoT devices today are either powered by batteries — which don’t all lose power at the same time and end up in landfills as toxic e-waste — or by cumbersome charging cables and cords that bring with them logistical nightmares, limited flexibility in designs, and hidden costs to IT teams managing large-scale IoT deployments. For these deployments to truly be effective and successful, we must remove the unnecessary reliance that many of today’s IoT devices have on wires, power cables, and replaceable batteries that are not only stunting IoT deployments but gaming our environment.

Welcome to the rise of wireless power networks, an ecosystem of technologies including transmitters and receivers that enable wireless power transmission across any distance for a wide range of applications for the billions of IoT devices today and the billions more of tomorrow whose power
needs are increasing. Wireless power networks can be particularly effective for retail and industrial settings, both of which can feature countless internet-connected sensors inside a single building, each often reliant on replaceable batteries or wires for power.

Consider a large retail store, which may have thousands of electronic shelf labels (ESLs) displaying prices. A more efficient option than paper labels, ESLs require constant power to function, and those with batteries do not all need replacing at the same time. Imagine the headaches that come with having to walk through aisle after aisle testing and replacing thousands of tiny batteries on a regular basis.

Today’s automated factories and warehouses are also increasingly equipped with IoT sensors for a wide range of uses, most of them still powered by yesterday’s technology (replaceable batteries and wires) despite being deployed for 21st century uses. Without a reliable, consistent, and streamlined power source, these deployments may fail to reach their full scale and potential, an ominous cloud for the broader IoT ecosystem that often overlooks this fundamental need.

Wireless power networks can also support enhanced data processing for edge IoT devices, providing these low-power devices with increased abilities to gather, process, and communicate data — such as their location — via artificial intelligence, providing additional functionality to IoT deployments.

Energous has been working to solve this challenge facing the expanding IoT ecosystem. Its WattUp technology — which is regulatory-certified in the U.S., Canada, the EU, China, and India — is capable of charging multiple devices simultaneously at a distance, sending RF-based wireless power to IoT deployments with thousands of devices at various transmit power levels. This provides unlimited coverage distance for IoT deployments, creating wireless power networks with reliable, consistent power levels that remove the need to rely on wires or manage and change out batteries.

Wireless power networks can help remove the reliance on charging wires and replaceable batteries while simultaneously aggregating IoT device data transfer to the cloud. When we free tomorrow’s IoT in these ways, we open up a world of flexible and mobile deployment with unlimited potential.

Reference

▶ PowerUP Expo (June 28–30, 2022)
Enabling High Power Density and Efficient Systems with GaN

By David Snook, manager of GaN products at Texas Instruments

Gallium nitride is a popular topic in the power electronics industry, as it enables highly efficient designs for applications such as telecom power supplies; electric vehicle charging; heating, ventilation, and air conditioning; appliances; and consumer power adapters. In industrial applications, GaN replaces traditional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), given its ability to drive higher power density and efficiencies as high as 99% for totem-pole power-factor correction (PFC). But because of its electrical properties and the performance that it enables, designing with GaN comes with a different set of challenges than silicon or even other wide-bandgap technologies, such as silicon carbide.

GaN VERSUS SiC

While there is some overlap in the power levels that GaN and SiC serve, GaN has fundamental characteristics that make it a better fit for applications in which high power density is critical in
In these applications, GaN devices can achieve switching frequencies of >150 kHz in PFC topologies and >1 MHz in DC/DC power converters, enabling a significant reduction in the size of magnetics in the system. By enabling higher switching speeds than SiC, GaN technologies help you achieve higher power density at a lower cost. Figure 1 illustrates a comparison of different technologies based on their power and operating frequency capabilities.

LEVERAGING A GaN FET FOR INDUSTRIAL APPLICATIONS

Each GaN power switch must be paired with an appropriate gate driver; otherwise, you may experience a pop and puff of smoke when testing at the bench! GaN devices can have uniquely sensitive gates, as they are not classical MOSFETs but are instead high-electron-mobility transistors (HEMTs). The cross-section of a HEMT, shown in Figure 2, appears similar to a MOSFET. But instead of current flowing through the full substrate or buffer layer, current flows through a two-dimensional electron gas layer.

Incorrect gate control of a GaN FET will cause a breakdown of the insulative layer, barrier, or other structural elements; the device will not only fail during that system condition, but it is likely also permanently damaged. This level of sensitivity necessitates a review of different types of GaN devices and their broad needs. HEMTs also do not have the traditional doped FET structure that forms p-n junctions, which then cause body diodes. This means that there are no internal diodes that can break down or cause unwanted behavior during operation, such as reverse recovery.
GATE DRIVER AND BIAS SUPPLY CONSIDERATIONS

Enhancement-mode (e-mode) GaN FETs look very similar to the e-mode silicon FETs with which you may already be familiar. A positive voltage of 1.5 V to 1.8 V will begin turning on the FET, with most operating conditions specified for 6-V gate threshold operation. However, most e-mode GaN devices have a maximum gate threshold of 7 V, which when violated will likely result in permanent damage.

If traditional silicon gate drivers do not offer proper voltage regulation or cannot handle the high common-mode transient immunity in a GaN-based design, many designers choose a gate driver such as the Texas Instruments (TI) LMG1210, which is designed specifically for use with a GaN FET. The LMG1210 offers a gate drive voltage of 5 V, regardless of supply voltage. Traditional gate drivers need very tight regulation of the gate driver’s bias supply so that they do not overstress the GaN FET. A cascode GaN FET, shown in Figure 3, is a compromise for ease of use compared with e-mode GaN FETs.

The GaN FET is a depletion-mode (d-mode) device, which means that it is normally on and requires a negative gate threshold to turn the device off. This is extremely problematic for a power switch, so most manufacturers add a 30-V silicon FET in series with the GaN FET for sale as one package. The gate of the GaN FET connects to the source of the silicon FET and applies the turn-on and turn-off gate pulses to the gate of the silicon FET.
Having a traditional isolated gate driver such as TI’s UCC5350 drive the silicon FET eliminates many gate driver and bias supply concerns. The biggest downsides of cascode GaN FETs are the higher output capacitance of the FET and susceptibility to reverse recovery, given the presence of a body diode. The output capacitance of the silicon FET adds on to that of the GaN FET, resulting in a 20% increase, which means >20% increased switching losses compared with other GaN solutions. And during reverse conduction, the body diode of the silicon FET conducts current and undergoes reverse recovery when the voltage polarity flips.

Cascode GaN FETs operate at slew rates of 70 V/ns (compared with 150 V/ns for other GaN solutions) to guard against avalanche breakdown of the silicon FET, increasing switching overlap losses. Although cascode GaN FETs are simpler to design with, they limit the achievable performance.

**INTEGRATION OFFERS AN EASIER SOLUTION**

The integration of a gate driver with built-in bias supply regulation and a d-mode GaN FET solves many of the design challenges of e-mode and cascode GaN FETs. For example, TI’s LMG3422R030, a 600-V 30-mΩ GaN device, has an integrated gate driver and power management features that enable higher power density and efficiency while reducing the risks and engineering effort required. Because the GaN FET is d-mode, there is a silicon FET integrated in series with the GaN FET. But the big difference versus cascode GaN FETs is that the integrated gate driver can directly drive the gate of the GaN FET, while the silicon FET performs the role of a normally off enabled switch at power-up. This approach, known as direct drive, eliminates the most pressing issues of cascode GaN FETs, such as higher output capacitance, reverse-recovery susceptibility, and avalanche breakdown of the silicon FET in series. The gate driver integrated in the LMG3422R030 enables very low switching overlap losses, enabling this GaN FET to operate at a switching frequency as high as 2.2 MHz and eliminating the risk of pairing the GaN FET with the wrong gate driver. Figure 4 shows an example of a half-bridge configuration using integrated LMG3422R030 GaN FETs.
The integrated driver shrinks solution size, enabling a power-dense system. Integrating a buck-boost converter also means that the LMG3422R030 can operate with a 9-V to 18-V unregulated power supply, which significantly reduces bias supply requirements. To enable a compact and lower-cost system solution, you could combine the LMG3422R030 with a ultra-low-electromagnetic-interference transformer driver such as TI's UCC25800, which has open-loop inductor-inductor-capacitor control with multiple secondary-side windings. Alternatively, a highly integrated, compact bias power supply such as TI's UCC14240 DC/DC module can supply the device locally, resulting in a low-profile design with a small printed-circuit-board footprint.

CONCLUSION
With the right gate driver and bias supply, GaN devices can help you achieve system-level benefits such as a switching speed of 150 V/ns, reduced switching losses, and a smaller magnetics size for high-power systems across industrial and automotive applications. Integrated GaN solutions simplify many of your device-level challenges so that you can focus on the wider system.

References

► **PowerUP Expo June 2022**

► **Optimizing GaN performance with an integrated driver**

► **Direct-drive configuration for GaN devices**

► **Understanding the Trade-offs and Technologies to Increase Power Density**
Motor Drive ICs Use Built-In System Fault Diagnosis to Reduce Field Returns

*BridgeSwitch combines high efficiency, design flexibility, enhanced safety, IEC 60335-1, and IEC 60730-1 compliance, with fault diagnosis.*

*By Cristian Ionescu-Catrina, senior product marketing manager at Power Integrations*

Designers are increasingly challenged by demands for continuous improvements in the efficiency and reliability of motor drives in consumer appliances. From the European Union to China, higher efficiencies are required for a growing range of consumer appliances, including dishwashers,
refrigerators, and heating, ventilation, and air conditioning (HVAC) systems. Designs are also required to comply with IEC 60335-1 and IEC 60730-1 safety requirements.

At the same time, consumers and manufacturers alike are demanding higher levels of reliability — less field service and fewer returns. According to a recent industry study, misdiagnosis results in 30% of compressor returns having ‘no fault found,’ adding to costs and inefficiencies across the supply chain and resulting in unhappy consumers. Harnessing the IoT can enable remote monitoring of consumer appliances, but the design must support meaningful and cost-effective fault diagnostics and protection functions.

To address these challenges, designers can turn to Power Integrations' family of BridgeSwitch, high-voltage, self-powered, half-bridge motor driver ICs with integrated protection, system monitoring, and reporting that deliver higher efficiency, increased design flexibility, and enhanced inverter and system reliability (Figure 1).

![Figure 1: BridgeSwitch combines high efficiency with extensive fault monitoring and reporting (blue text) for increased system and inverter reliability](image)

**HIGH EFFICIENCY SIMPLIFIES THERMAL MANAGEMENT**

BridgeSwitch integrated half-bridges simplify the development and production of high-voltage, inverter-driven, single- or three-phase permanent magnet or brushless DC motor drives. BridgeSwitch ICs include a proprietary instantaneous phase current output signal that facilitates the design of sensor-less control schemes. These ICs include two 600-V, N-channel power FREDFETs, with
high- and low-side drivers, in a small-outline, surface-mount package (13.6 × 9.4 × 1.35 mm) that offers extended creepage distances and allows cooling of both power FREDFTs via the printed circuit board (Figure 2).

Figure 2: This bottom view of the BridgeSwitch InSOP-24C package shows the extended creepage distance (lower right) and the cooling pads for the high- and low-side FREDFTs

The ultrasoft and ultrafast diodes in the FREDFTs are optimized for hard-switched inverter drives. The high- and low-side control and drivers are self-supplied, eliminating the need for an external auxiliary power supply. The distributed thermal footprint, combined with up to 99.2% efficiency, eliminates the need for an external heatsink at rated continuous RMS current, reducing system cost, size, and weight. BridgeSwitch ICs can deliver up to 400 W of output power and are well-suited for use in inverters in appliances such as dishwashers and refrigerators and for the condenser fans in high-efficiency air conditioners.

HARDWARE-BASED FAULT PROTECTION SAVES CERTIFICATION COST AND TIME

The microcontroller (MCU) in most inverter designs is used to monitor and react to fault conditions, as well as controlling the motor. Motor control is straightforward and relatively quick to implement using standard software packages. Fault diagnostics and protection are more challenging and can vary significantly from one application to another, as they rely on a variety of different sensors to monitor the phase currents, system overtemperature conditions, vibration, and other system
parameters. It is complex to program the MCU to interpret the sensor inputs and implement protection in the appropriate manner needed to gain certification to international standards.

Certifying the monitoring and control software is a time-consuming and costly process, often delaying time to market. On the other hand, the hardware-based motor fault protection in BridgeSwitch ICs is compliant to the abnormal motor operation requirements of IEC 60335-1 and IEC 60730-1 without relying on software to control, reducing costs and speeding time to market. The resulting ability to use Class A software designation per IEC 60730-1 can save two months of certification time, and the use of BridgeSwitch ICs also simplifies the safety approval process for product software updates.

BridgeSwitch combines comprehensive internal fault protection functions with external system level monitoring and reporting via a bidirectional fault bus (Figure 3). Internal fault protection includes two-level thermal overload protection and hardware programmable cycle-by-cycle over-current protection for both FREDFETs. System-level monitoring includes four undervoltage levels and one overvoltage level on the high-voltage DC bus, and external sensors such as a negative-temperature-coefficient temperature sensor, a vibration sensor, and the ability to detect a stalled motor, disconnected motor phase, or running overload.

The single-wire fault bus is based on an open-drain architecture and enables the BridgeSwitch ICs to send status updates using an 8-bit word, with the eighth bit providing odd parity to ensure signal
Motor Control

integrity. It is also used by the MCU to send:

- Commands to the BridgeSwitch ICs
- Queries to the BridgeSwitch ICs for status updates
- Reset commands to ICs that are latched off for an overtemperature fault

The ID pin is used at power up to set a unique IHB identification for each BridgeSwitch IC, enabling the MCU to identify which IC provided a given fault alert: IHB1 has the ID pin connected to BPL, the ID pin is floating for IHB2, and the ID pin is connected to SG for IHB3 (Figure 4). In addition, setting the IHB identification of each IC supports arbitration on the single-wire bus using the device ID time period (t_{ID}). HB1 has a t_{ID} of 40 µs, the t_{ID} for HB2 is 60 µs, and the t_{ID} for HB3 is 80 µs. The system MCU is assigned a default t_{ID} of 160 µs, guaranteeing that it always wins bus arbitration.

**MOTOR-EXPERT SUITE ACCELERATES TIME TO MARKET**

Power Integrations’ Motor-Expert Suite of software features speed and current control-loop functions and includes an embedded C code application, library, and control GUI that supports single-phase and three-phase designs using BridgeSwitch ICs. It accelerates time to market by

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*Figure 4: BridgeSwitch status reporting combines single-wire fault communication bus with device ID programming (green)*
providing a graphical interface to all parameters and commands, as well as a terminal emulator for interacting with the motor controller in serial mode. The Motion Scope window displays real-time linear graphs of controller variables. New functions and use cases can be added and users can easily port the software to an MCU. The software needs only 14 kB of code memory and 5 kB of SRAM, making it suitable for running on MCUs with limited memory resources. Software developed using Motor-Expert meets static (MISRA) and dynamic performance requirements for latency, jitter, and execution time.

CONCLUSION
Designers can turn to BridgeSwitch ICs with built-in system fault diagnosis to reduce field returns and speed time to market. These self-powered, half-bridge motor driver ICs deliver the high efficiency, design flexibility, and enhanced inverter and system reliability demanded in modern consumer appliances. The extensive hardware-based protection functions save certification time and costs. These ICs are IEC 60335-1– and 60730-1–compliant, as confirmed in UL Report 4788685352. The ID pin enables the MCU to pinpoint the location of faults. Finally, the use of Motor-Expert design software further speeds time to market for single-phase and three-phase applications of BridgeSwitch ICs.

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Compact Size of Motor Drive with GaN Chips for eBikes and Drones

The reference design of the EPC9173 GaN-based inverter optimizes motor drive system size, performance, range, precision, and torque, all while promoting simplicity in the design for quicker time-to-market. The compact size of this inverter enables integration into the motor housing resulting in the lowest EMI, highest density, and lowest weight.

Report Reveals Investors’ Views on Unlocking the Hydrogen Economy

The European Investment Bank (EIB) has recently released a report on investor viewpoints on how the public sector can best support in addressing the risks and challenges associated with the transition to a hydrogen-fueled economy. The European Investment Bank is the long-term lending institution of the European Union owned by its Member States.

AnyPort Simplifies Multi Port Chargers Design

Silanna Semiconductor has recently announced the release of AnyPort, a breakthrough new architecture that allows designers to complete a charger design for a specified power level before selecting and setting the output ports. The AnyPort architecture for multiport chargers will be made available for a wide range of silicon- and GaN-based designs enabling power levels more than 100W.

Patent Application for Simplified Onboard EV Charging Solution

Hillcrest Energy Technologies, a clean technology company developing transformative power conversion technologies and control system solutions for next-generation electrical systems, announces the company has filed a patent application for a simplified EV charging solution. Initial proof-of-concept lab testing confirms the ability of the enhanced power-train solution to provide universal, backward compatible, bidirectional...
PCIM has hosted a lot of companies that are playing to the sound of GaN and SiC, but not only. Semiconductors for electric vehicles, the energy revolution, all these are part of an ecosystem that is evolving at a fast speed.

PowerUP Expo is a Virtual Conference and Exhibition with the goal of envisioning the future of power electronics. It will take place June 28–June 30.

In several energy industries, the silicon carbide (SiC) industry is expanding to provide highly efficient and Silicon carbide (SiC) is expanding in several energy industries to deliver extremely efficient and compact solutions.

Guy Moxey, Senior Director of Power Marketing at Wolfspeed, has spent his entire career in the power semiconductor industry with roles in applications, product marketing...
Electrochemical Impedance Spectroscopy (EIS) for Batteries

This circuit note describes an electrochemical impedance spectroscopy (EIS) measurement system for characterizing lithium ion (Li-Ion) and other types of batteries. EIS is a safe perturbation technique used to examine processes occurring inside electrochemical systems.

Power saving methods for LTE-M and NB-IoT

LTE-M and NB-IoT require long battery lifetime to ensure IoT services and minimize maintenance costs in the future. This technical white paper describes the possible power saving methods that can be applied to LTE-M and NB-IoT devices.

GaN and SiC, Devices and Technology – Download our eBook

Improved energy efficiency and growing demand for longer battery life are prompting the power electronics community to take yet another hard look at the tradeoffs presented by wide-bandgap semiconductor technology operating at higher voltages, temperatures, and frequencies.

Can You Really Get ppm Accuracies from Op Amps?

Commercially available ppm-accurate amplifiers are difficult, if not impossible, to find. This article presents op amp accuracy limitations and how to choose the few op amps that have a chance of 1 ppm accuracy. It will also discuss a few application improvements to existing op amp limitations.

The Power Electronics News & Know-how e-mail newsletter

 informs about Products, Technologies, Applications and technical Trends about Power Supplies, Power Components, Thermal Management and more.